The MEDEA Design Automation Roadmap: Design Automation Solutions for Europe

by
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The semiconductor industry has been growing at an unprecedented rate since its start in the early 1960s, capitalising on the outstanding properties of silicon and its stable oxide, allowing the advent of the CMOS industry, the leading process of the whole semiconductor industry. The average semiconductor sales growth of 15% - 16% per year has been raising tremendous problems of huge investments in manufacturing. A rapid return of investment through advanced products (in the latest available processes) having high added value at system level is mandatory. Sometimes the system is the product itself and this raises the question of new methods to design such complex systems on a single chip mixing several functionalities.

The following Roadmap is a forecast of what could be the European evolution of design automation, with the present status of its lack of local industrial developments but a tremendous reservoir of knowledge. It provides a way of paving the road to new design solutions and truly providing capability to influence US developments as is evidenced by frequent technology partnerships with US software vendors. Recently a significant increase of European start-ups in advanced design automation domains (HW – SW co-design, IP re-use, Deep Submicron effects...) has been seen.

However it should be recognised that the evolution to system on a chip capability in silicon has been mostly analysed through silicon process evolution which is an ENABLER at the same level as design automation, the end product being the silicon chip itself that sells on the market. The early accessibility of products in the latest silicon is key for the maturity of these processes and Europe is lagging behind the US though process development is often in well aligned. One strategic objective of Europe should be to contribute to engineer more rapidly the design solutions, in various SILICON APPLICATION PLATFORMS of choice to be able to develop early REUSABLE SYSTEM IP's for the next generation of products. These system IP's will include basic digital functions but also added value functionality like analogue (a long lasting European recognised expertise), RF, embedded memories (SRAM, DRAM, Non volatile) micro mechanical functions…

The semiconductor industry, during the past 30 years, has grown so fast that its "process" maturity has not been equalled globally. Manufacturing is highly efficient and predictable, design automation lacks engineering and performance. This is a major bottleneck to use the full possibilities of the silicon process available today.

The Application group of MEDEA therefore started the Design Automation Roadmap activity the main results of which are shown in this article: the flow and the overall roadmap. This roadmap gives targets, appropriate to Europe, to contribute to bridge this gap.

The roadmap addresses the topics mentioned above and will give a targeted evolution up to 2004 where we still have a good visibility of what can be influenced. In this roadmap European specifications are stressed in terms of:

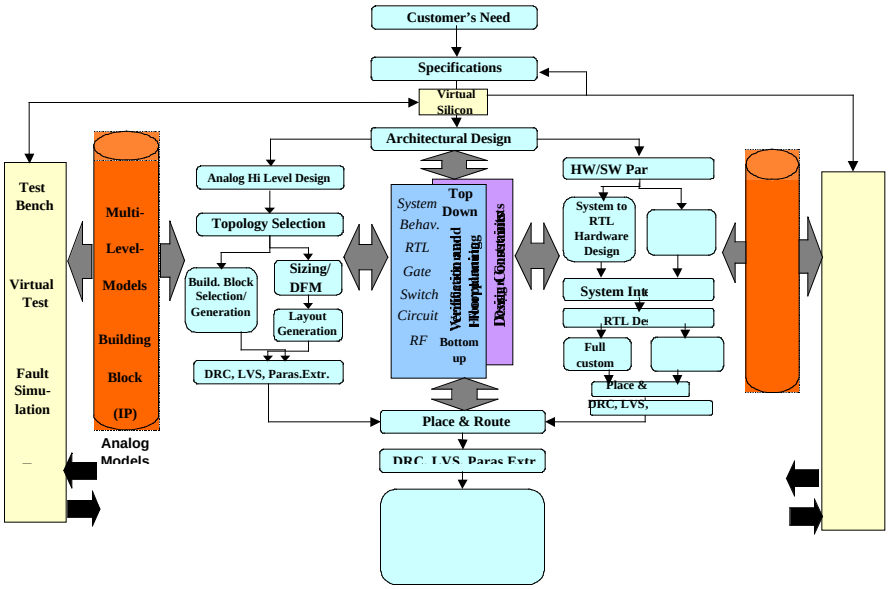
- Strong analogue-digital culture (including RF).
- System level knowledge specificity shared from past European co-operative programs.
- IP's as an urgent and mandatory approach to create a step function increase in design efficiency and to be integrated in the Silicon System Design Platforms at higher levels of complexity.
- Back end as an engineered flow integrating deep submicron effects (crosstalk…).
- Top down verification starting from system description.

The general architecture of the mixed analogue / digital design and test flow is given in Figure 1 where on the backbone of the digital flow starting from specification validation with the customer to the final packaging are added:

- The analogue and mixed analogue digital flow on one side.
- The IP reuse and the test solutions on the other side.
- All the above steps are to be considered in an efficient verification environment at the level of the complexity of the problem: from higher description levels (C, C++) down to single gate behaviour.

To illustrate the roadmap the following definitions are considered:

- Research; this covers the early appearance of the concept and the



demonstration of feasibility on demonstrators.

- Development means that research results are believed to be applicable to solve problems, breakthroughs in the evolution of Electronic Design Automation capabilities. They should either be developed internally by European companies (system or semiconductor) to get earlier benefit of their impact on the business or developed in co-operation with major software vendors, or these solutions could initiate new start-ups.
- Quality/production ensures that the solution is production proof, has been fully debugged and can be supported.

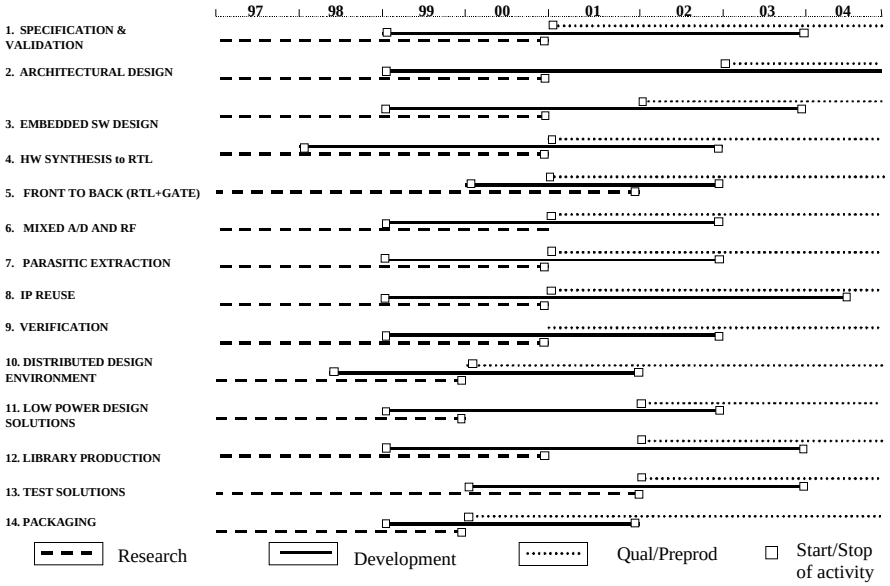
The various ingredients of the roadmap are shown in Figure 2 where forecast time frames of appearance are given: the major topics are listed vertically in much the same order as they would appear in a design flow. The horizontal axis gives the maturity time frame of the solutions as seen today. New contents will appear when bottlenecks show up and will be introduced when and where necessary.

All the 14 topics of the roadmap are described in detail in a booklet "The MEDEA Design Automation Roadmap" which can be ordered via the MEDEA homepage:

www.medea.org

We regard this first release as a live document to start the discussion with all interested people. We invite you cordially to contribute via ECSI or MEDEA.

2 - MIXED ANALOG/DIGITAL SILICON SYSTEM DESIGN AND TEST FLOW ROADMAP (DATES OF COMPLETE SOLUTION FIRST APPEARANCE)



Major efforts should be made in four main areas:

- Consolidate the Design Automation Technology in areas such as IP's (Intellectual Property) system blocks for greater system knowledge reuse, HW – SW Co-design and Deep Submicron Back-end and verification (60% – 70% of design time).
- Set up system level design solutions, including virtual silicon capability for early prototyping.
- Target a one month design cycle in silicon system platform solutions covering focused markets on which most of the software and IP developments can be reused.
- Make an in-depth effort to engineer the Design Automation solutions following the example of what has been done in the silicon process.

It is believed that Europe can take such a challenge thanks to:

- An existing tradition of co-operation.
- A high level of maturity in silicon production.
- Deep knowledge and expertise in design automation issues.

MEDEA EDA Roadmap Workshop

Nice, Côte d'Azur, France
November 18th, 1999
Organized by ECSI and MEDEA

The workshop will enable a common discussion and working forum on the EDA Roadmap for all industry sectors. It will give an overview of the background and the present status of the EDA Roadmap as well as future directions of its evolution. The parallel sessions will be organised to correspond to the sections of the roadmap.

Agenda

10:00-10:15	**Introduction** *Anton Sauer (MEDEA)*
10:15-10:45	**General presentation** *Joseph Borel, (ST Microelectronics)*
10:45-12:30	**Short presentation by the scheme owners** (14 5-minute presentations giving the coverage of sebsections VI-X of the Roadmap)
12:30-14:00	Lunch
14:00-15:30	**14 Parallel workshop sessions** managed by the scheme owners
15:30-17:00	**Presentations of the conclusions** by each scheme owner
17:00	Close

For registration or supplementary information contact the ECSI Office:

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